REMARKS

The office action of November 8, 2005 has been reviewed and its contents carefully noted. Reconsideration of this case, as amended, is requested. Claims 1 through 28 remain in this case, claims 1 and 10 being amended, and claims 11 through 28 being added by this response.

No new matter has been added. More specifically, claims 11, 22, 23 and 25 are fully supported by page 3, lines 10-18, page 3, lines 21-25, page 8, lines 15-22, Figs. 2(e) and 2(f) and claim 1, as filed. Claims 12 through 20 are fully supported by claims 2 through 10, as filed. Claims 21, 24 and 26 are fully supported by claim 1, as filed. Claims 27 and 28 are fully supported by page 3, lines 13-28 and claim 1, as filed.

Although the Applicant is not submitting a declaration at this point, the Applicant is submitting a Supplemental Information Disclosure Statement along with this response. The Applicant respectfully requests that the Examiner note that the present invention has since been published in these well-known and respected journals, and presented as invited talks at leading international conferences. The invention has received notoriety as an important and novel discovery. This is evidence of the novelty of the invention and that it is widely regarded as groundbreaking technology. The references also illustrate the long-felt need for this technology. Those of ordinary skill in the art recognize the importance of the discovery. The Applicant believes that this evidence stands, on its own, without the need for a declaration. The Applicant would request the opportunity to file a declaration, if the Examiner is not convinced of the notoriety and import of publication within these specific journals and invitations to the conferences regarding this invention. The Applicant would also appreciate the opportunity to schedule an interview, either telephonic or in person, with the Examiner, if an interview would further prosecution of the application.

The numbered paragraphs below correspond to the numbered paragraphs in the Office Action.

Rejection under 35 U.S.C. §103

4. Claims 1-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tadatomo et al. Applicant respectfully disagrees.

Tadatomo discloses "[a] GaN group crystal base member comprising a base substrate, a mask layer partially covering the surface of said base substrate to give a masked region, and a GaN group crystal layer grown thereon to cover the mask layer, which is partially in direct contact with the non-masked region of the base substrate, use thereof for a semiconductor element, manufacturing methods thereof and a method for controlling a dislocation line. The manufacturing method of the present invention is capable of making a part in the GaN group crystal layer, which is above a masked region or non-masked region, have a low dislocation density". (Abstract, see also Summary, Col. 1, lines 54-59) The mask layer is necessary in Tadatomo.

In contrast, the present invention discloses "[a] method of *in-situ* fabrication of dislocation-free structures from plastically relaxed layers grown on a semiconductor surface suitable for epitaxial growth is disclosed. This method solves the problem of lattice-mismatched growth." (present application, page 3, lines 5-7).

Using a mask in Tadatomo includes necessarily patterning a substrate by means of lithography. Patterning is explicitly mentioned in the Tadatomo. "The present inventors previously proposed forming mask layers 2 having a lattice pattern on a base substrate I to avoid cracks...." (Col. 3, lines 38-40) The fabrication of a mask as shown explicitly in Figs 1 through 6 includes fabrication of a periodic pattern on a substrate. "The mask layer 2 may have any pattern such as a lattice pattern, a stripe pattern and a dot pattern." (Col. 4, lines 43–44).

In the present application, there is no lithographic process such as deposition of a mask. Instead, the present application uses an epitaxial approach. "The method produces coherent dislocation–free regions from initially dislocated and/or defect–rich layers lattice mismatched with respect to the underlying substrate, which does not contain any processing step before or after formation of defect–free regions". (present application, page 3, lines 13-16).

The present invention "preferably uses in situ formation of a cap layer on top of a dislocated layer. The cap layer preferably has a lattice parameter close to that in the underlying substrate, and different from that in the lattice mismatched epilayer in the no–strain state. Under these conditions, the cap layer undergoes elastic repulsion from the regions in the vicinity of the dislocations, where the lattice parameter is the most different from that in the substrate. The cap layer is absent in these regions." (present application, page 3, lines 16-21). Absence of the cap layer in the regions in the vicinity of the dislocations is the direct consequence of the elastic repulsion of the cap layer material from the regions in the vicinity of the dislocations.

Figs. 1(e) and 1(f) of the present application specifically show a layer that has trenches (5) once defect-rich regions have been eliminated. These trenches (5) are preferably filled in if an additional layer (6) is grown on the structure. Tadatomo et al. does not remove any dislocations, and consequently does not have the trench structure (5) shown in Fig. 1(e) or the filled in structure shown in Fig. 1(f). Instead, Tadatomo covers a substrate by a mask. "The surface of the base substrate 1 is partially covered by mask layer 2, and the GaN group crystal layer 3 grows from the non–masked region 11 of the base substrate 1 and covers the mask layer 2" (Col. 4, lines 7–11). As far as the Applicant knows, none of the prior art teaches or suggests the resulting structure shown in Fig. 1(f).

Another embodiment Tadatomo et al. includes alternates periodic repetition of masked and non–masked regions aimed to block propagation of dislocations upwards. "The GaN group crystal base member of claim 3, wherein a masked region and a non–masked region are alternately repeated periodically ..." (Claim 4, Col. 17, lines 42–44).

In contrast, the present invention includes an annealing step resulting in the removal of material containing dislocations. "When a cap layer has a lower thermal evaporation rate than the underlying lattice–mismatched layer, the regions of this lattice–mismatched layer are selectively evaporated at high enough temperatures, and only the coherent defect–free regions of the initially defect–rich lattice–mismatched layer remain on the substrate". (present application, Abstract, see also the Summary of the Invention).

Further, the difference between the two inventions is clearly seen from the Figures. In Tadatomo et al. dislocations remain in the structure (Figs. 1(a), 1(b), and 4), they are just blocked

by the mask. In the present invention, dislocation–contained regions are removed by evaporation (Fig. 2, the evaporation transforms Fig. 2(d) into Fig. 2(e)).

The materials in the device of the present invention have different thermal evaporation rates. Evaporation of uncovered dislocated regions is important in the present invention; thus, the proper selection of materials with certain thermal evaporation rates is also important. In contrast, Tadatomo does not teach or suggest relationships between the thermal evaporation rates of the materials used.

The materials of the device of the present invention also have relationships between their lattice constants. Selective growth in the present invention occurs not due to the chemical difference between the materials, but due to the different strain state in the vicinity of the dislocations and far from the dislocations. Selective evaporation occurs due to a difference in thermal evaporation rate of the materials having rather similar chemical natures.

In contrast, Tadatomo et al. imposes a strong restriction on the mask material. "Said base substrate allows growth of a GaN group crystal in the C axis orientation as the thickness direction, and the mask layer is made from a material substantially free from GaN group crystal growth" (Col. 1, lines 59–63).

Regarding claim 1, the Examiner acknowledges that Tadatomo et al. does not specifically disclose the method steps claimed. However, the Examiner further states that there "is not any non-obviousness difference between the two final products." (present office action dated November 8, 2005, page 3, lines 9-10).

The Examiner states that Tadatomo et al. discloses a lattice-mismatched layer having at least one local dislocation.

> "In the GaN group crystal base member of the present invention as shown in the embodiment of FIG. 1, the surface of the base substrate 1 is partially covered by mask layer 2, and the GaN group crystal layer 3 grows from the non-masked region 11 of the base substrate 1 and covers the mask layer 2.
>
> The material of the above-mentioned base substrate 1 may be, for example, sapphire crystal (C face, A face), rock crystal, SiC and the like which are widely used to

form GaN group crystal layers. In particular, sapphire substrate (C face) is preferred. The substrate may have a buffer layer of ZnO, MgO, AlN and the like on its surface to reduce the difference in the lattice constant and coefficient of thermal expansion between the substrate and GaN group crystal layer. In addition, a material having a thin layer of $In_x Ga_yAl_zN$ ($0 \leq X \leq 1$, $0 \leq Y \leq 1$, $0 \leq Z \leq 1$, $X+Y+Z=1$) such as GaN or GaAlN formed on said buffer layer may be appropriately used. Such base substrate can reduce the density of the dislocation newly generated from the non-masked region into a GaN group crystal layer 3 and afford a GaN group crystal layer 3 having fine crystallinity.

The mask layer 2 should be one, from which surface a GaN group crystal does not substantially grow. Examples of such material include non-crystalline materials such as nitrides and oxides of Si, Ti, Ta, Zr and the like, namely, SiO_2, SiN_x $SiO_{1-x}N_x$, TiO_2, ZrO_2 and the like. In particular, SiO_2, SiN_x and $SiO_{1-x}N_x$ are suitable which are superior in heat resistance and which allow relatively easy film formation and removal by etching. These materials may be formed into a multilayer structure". (col. 4, lines 6-36)

Figs 1a, 1b, and Fig12a in Tadatomo all show a GaN layer including dislocations. Tadatomo does not teach or suggest any of those dislocations being eliminated; all of the dislocations in the original GaN layer are still present in the final product. All of the dislocations remain in the structure (see Figs. 1(a), 1(b) and 4), they are just covered by the mask.

In contrast, in the product of the present invention, at least one dislocation is eliminated by local evaporation of the nearby region of the lattice-mismatched layer in the lattice-mismatched layer that originally has at least one local dislocation. Therefore, the final product in claim 1 is different from the product in Tadatomo, in that the dislocations in the lattice-mismatched layer have been eliminated in the lattice-mismatched layer of claim 1. This is a non-obvious and important difference. As discussed in the present application, "[t]he method produces coherent dislocation-free regions from initially dislocated and/or defect-rich layers lattice mismatched with respect to the underlying substrate, which does not contain any processing steps before or after formation of the defect-free-regions." (present application, page 3, lines 8-11).

Claim 1 includes, in part, "such that the <u>cap layer nucleates selectively on at least one region of the lattice-mismatched layer</u> such that the <u>at least one dislocation is not covered by the</u>

cap layer." (emphasis added) Tadatomo does not teach or suggest a structure with a cap layer that nucleates selectively so that it does not cover at least one dislocation.

Claim 1 also includes, in part, the step of "c) annealing the device at a temperature and duration, such that the at least one dislocation is eliminated by local evaporation of the nearby region of the lattice-mismatched layer". (emphasis added). Tadatomo does not teach or suggest a device that has a dislocation-eliminated layer. As discussed above, no dislocations are eliminated in Tadatomo.

The Examiner states that "Tadatomo shows obtaining a device having a low dislocation density and shutting off the extension of the dislocation (eliminating)" (present office action dated November 8, 2005, page 4, lines 19-20). The Examiner points to the following passages to support this statement.

"A GaN group crystal base member comprising a base substrate, a mask layer partially covering the surface of said base substrate to give a masked region, and a GaN group crystal layer grown thereon to cover the mask layer, which is partially in direct contact with the non-masked region of the base substrate, use thereof for a semiconductor element, manufacturing methods thereof and a method for controlling a dislocation line. The manufacturing method of the present invention is capable of making a part in the GaN group crystal layer, which is above a masked region or non-masked region, have a low dislocation density". (Abstract) This passage merely states that the patent discloses a method for controlling a dislocation line, not a method for eliminating dislocations/defects. It also states that the GaN group crystal layer has a "low dislocation density", but again there is nothing in this passage teaches or suggests the elimination of defects, or a defect-eliminated layer.

> "However, the crystal growth of a GaN semiconductor material to give a thick film results in tremendous amounts of stress applied on the interface between GaN and sapphire substrate due to different lattice constants and coefficients of thermal expansion, which in turn leads to a problem in that GaN is broken and a bulky substrate cannot be obtained. In addition, this method produces only a substrate having an extremely great dislocation density (e.g., $1x10^9$ cm^{-2} -$1x10^{10}$ cm^{-2}). By dislocation is meant here a defect that occurs when a semiconductor layer is grown on a substrate under a lattice mismatch.

The dislocation thus created advances upward along with the growth of the crystal layer and passes through an active layer to form a continuous defective portion called a dislocation line (continuous dislocation). Inasmuch as this dislocation is a crystal defect, it acts as a non-radiative recombination center or as a path of a current to ultimately induce current leakage when such GaN semiconductor material is used for a light emitting element, which in turn degrades light emitting performance and shortens the service life.

It is therefore an object of the present invention to provide a GaN group crystal base member having a low dislocation density." (col. 1, lines 22 to 44).

This passage explains some problems created when stress is applied on the interface between GaN and a substrate. The passage does not teach or suggest a device where at least one dislocation is eliminated.

"The non-dislocation as referred to in the present invention means not only the ideal state completely free of dislocation which is theoretically possible, but also the state considered to have sufficiently low dislocation density to the degree the influence of the dislocation may be ignored from the industrial aspect, when compared to the dislocation density in the case where a GaN group crystal is grown on a sapphire substrate via a buffer layer." (col. 3, lines 24-32). This passage defines "non-dislocation" with respect to the patent. In addition, "low dislocation density", as explained in this passage, <u>does not</u> mean dislocations have been eliminated, or that there is a dislocation-free layer.

"A semiconductor light emitting element such as LED and LD (laser diode) can be produced by forming a light emitting part comprising a cladding layer and an active layer, and electrodes on the GaN group crystal base member of the present invention, particularly, a GaN group crystal layer 3 grown thick.

As in the embodiment of FIG. 1, when a low dislocation density part is formed on the mask layer 2, occurrence of dislocation is not reduced in other parts. Thus, in the present invention, as shown in FIG. 4, the GaN group crystal base member (base substrate 1, first mask layer 2 and first GaN group crystal layer 3) shown in the above-mentioned FIG. 1 is used as a new base substrate M, on which a second mask layer 21 is formed in the same manner as in FIG. 1, thereby shutting off extension of the dislocation

line, and then a second GaN group crystal layer 31 is grown thereon. In this manner, a GaN group crystal base member almost without dislocation can be obtained. In FIG. 4, the dislocation lines linearly rise from the non-masked region.

The GaN group crystal base member obtained by forming the above-mentioned second GaN group crystal layer 31 is used as a new base substrate M, and a mask layer and a GaN group crystal layer may be repeatedly formed an optional number of times to form a GaN crystal having an almost non-dislocation state." (col. 5, lines 15-39)

This passage does not teach or suggest the elimination of at least one dislocation. The Examiner states that shutting off the extension of the dislocation is equivalent to eliminating a dislocation. However, shutting off the extension of the dislocation merely keeps the dislocation line from spreading. This is very different from eliminating existing dislocations.

In addition, the semiconductor device in claim 1 includes a surface having a first lattice constant and a first thermal evaporation rate, a lattice-mismatched layer, having a second lattice constant and a second thermal evaporation rate, and a cap layer having a third lattice constant and a third thermal evaporation rate. The second lattice constant is different than the first lattice constant. The third thermal evaporation rate is lower than the second thermal evaporation rate. Tadatomo does not teach or suggest any of these relationships in its device.

Since claim 1 includes one or more elements not taught or suggested in Tadatomo, claim 1 is not anticipated by Tadatomo. Reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

Claims 2-10, being dependent upon and further limiting claim 1, should also be allowable for that reason, as well as for the additional recitations they contain. Reconsideration and withdrawal of the rejection of claims 2-10 is respectfully requested.

In order to further prosecution of the application, the Applicant respectfully submits arguments regarding the differences between Tadatomo and new claims 11 through 22. The arguments regarding the obviousness of claim 1 are repeated herein by reference.

Regarding claims 11 and 23, the claims includes, in part, "a lattice-mismatched layer, having a second lattice constant in no-strain state, which is different than the first lattice

constant, wherein the lattice-mismatched layer has a second thermal evaporation rate, <u>and wherein the lattice-mismatched layer is free of dislocations</u>". Tadatomo does not teach or suggest a lattice-mismatched layer free of dislocations. In fact, Tadatomo acknowledges that the GaN layer includes dislocations.

In addition, the semiconductor structure in claims 11 and 23 includes a surface having a first lattice constant and a first thermal evaporation rate, a lattice-mismatched layer, having a second lattice constant and a second thermal evaporation rate, and a cap layer having a third lattice constant and a third thermal evaporation rate. The second lattice constant is different than the first lattice constant. The third thermal evaporation rate is lower than the second thermal evaporation rate. Tadatomo does not teach or suggest any of these relationships in its structure.

Therefore, claims 11 and 23 are not obvious over Tadatomo. Claims 12-20, being dependent upon and further limiting claim 11, should also be allowable for that reason, as well as for the additional recitations they contain.

Regarding claims 21 and 24, the claims include, in part, "annealing the semiconductor structure at a temperature and duration, such that the plurality of dislocations are eliminated by local evaporation of the nearby region of the lattice-mismatched layer". Tadatomo does not teach or suggest a lattice-mismatched layer where a plurality of dislocations in that layer are eliminated. In fact, Tadatomo acknowledges that the GaN includes dislocations.

In addition, the semiconductor structure in claims 21 and 24 include a surface having a first lattice constant and a first thermal evaporation rate, a lattice-mismatched layer, having a second lattice constant and a second thermal evaporation rate, and a cap layer having a third lattice constant and a third thermal evaporation rate. The second lattice constant is different than the first lattice constant. The third thermal evaporation rate is lower than the second thermal evaporation rate. Tadatomo does not teach or suggest any of these relationships in its structure. Therefore, claim 21 and 24 are not obvious over Tadatomo.

Regarding claims 22 and 25, the claims include, in part, "a lattice-mismatched layer, having a second lattice constant in no-strain state, which is different than the first lattice constant, wherein the lattice-mismatched layer has a second thermal evaporation rate, <u>and</u>

wherein the lattice-mismatched layer is free of dislocations". Tadatomo does not teach or suggest a lattice-mismatched layer free of dislocations. In fact, Tadatomo acknowledges that the GaN layer includes dislocations.

Claims 22 and 25 also include, in part, "annealing the semiconductor structure at a temperature and duration, such that the plurality of dislocations are eliminated by local evaporation of the nearby region of the lattice-mismatched layer". Tadatomo does not teach or suggest a lattice-mismatched layer where a plurality of dislocations in that layer are eliminated. In fact, Tadatomo acknowledges that the GaN includes dislocations.

In addition, the semiconductor structure in claims 22 and 25 includes a surface having a first lattice constant and a first thermal evaporation rate, a lattice-mismatched layer, having a second lattice constant and a second thermal evaporation rate, and a cap layer having a third lattice constant and a third thermal evaporation rate. The second lattice constant is different than the first lattice constant. The third thermal evaporation rate is lower than the second thermal evaporation rate. Tadatomo does not teach or suggest any of these relationships in its structure. Therefore, claims 22 and 25 are not obvious over Tadatomo.

Regarding claim 26, the claim includes, in part, "such that the cap layer nucleates selectively on at least one region of the lattice-mismatched layer such that the at least one dislocation is not covered by the cap layer." (emphasis added) Tadatomo does not teach or suggest a structure with a cap layer that nucleates selectively so that it does not cover at least one dislocation.

Claim 26 also includes, in part, the step of "c) annealing the device at a temperature and duration, such that the at least one dislocation is eliminated by local evaporation of the nearby region of the lattice-mismatched layer". (emphasis added). Tadatomo does not teach or suggest a device that has a dislocation-eliminated layer. As discussed above, no dislocations are eliminated in Tadatomo.

In addition, the semiconductor structure in claim 26 includes a surface having a first lattice constant and a first thermal evaporation rate, a lattice-mismatched layer, having a second lattice constant and a second thermal evaporation rate, and a cap layer having a third lattice

constant and a third thermal evaporation rate. The second lattice constant is different than the first lattice constant. The third thermal evaporation rate is lower than the second thermal evaporation rate. Tadatomo does not teach or suggest any of these relationships in its structure.

Regarding claims 27 and 28, the claims include, in part “wherein the lattice-mismatched layer includes at least one defect-free region and at least one defect-rich region that has been removed to eliminate dislocations.” Tadatomo does not teach or suggest a lattice-mismatched layer with at least one defect-free region and a removed-defect-rich region. As discussed above, no defects are eliminated in Tadatomo.

Claims 27 and 28 also include, in part, “a cap layer, having a third lattice constant and a third thermal evaporation rate, wherein the cap layer is absent from the defect-rich region that has been removed”. Tadatomo does not teach or suggest a structure with a cap layer that is absent from a defect-rich region that has been removed.

In addition, the semiconductor structure in claims 27 and 28 includes a surface having a first lattice constant and a first thermal evaporation rate, a lattice-mismatched layer, having a second lattice constant and a second thermal evaporation rate, and a cap layer having a third lattice constant and a third thermal evaporation rate. The second lattice constant is different than the first lattice constant. The third thermal evaporation rate is lower than the second thermal evaporation rate. Tadatomo does not teach or suggest any of these relationships in its structure.

Conclusion

Applicant believes the claims, as amended, are patentable over the prior art, and that this case is now in condition for allowance of all claims therein. Such action is thus respectfully requested. If the Examiner disagrees, or believes for any other reason that direct contact with Applicants' attorney would advance the prosecution of the case to finality, he is invited to telephone the undersigned at the number given below.

"Recognizing that Internet communications are not secured, I hereby authorize the PTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file."

Respectfully Submitted:
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